

An HEMT with an Integrated On-Drain Capacitor as Basis of an Hybrid Mixer

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Abstract— This paper reports the study of an HEMT, the characteristic of which is to have a decoupling capacitor directly integrated between its drain and source electrodes. It is shown that, with an appropriate design of this basic filtering element, such a device proves to be efficient as for the realization of hybrid gate mixers. An experimental demonstration of this property is given by the comparing a HEMT without capacitor with a HEMT with an integrated capacitor. For the latter, the gate length of which is $0.3\ \mu\text{m}$, it is shown that, at 18 GHz, a 5-dB improvement of conversion gain is provided by the integrated capacitor.

I. INTRODUCTION

IT IS WELL KNOWN that, in order to get the optimum performance of a FET gate mixer, the load impedance presented to the intrinsic drain needs to be a pure resistance at the IF frequency and a short-circuit at the RF and LO frequencies. The experience and the analysis of hybrid realizations have shown that, as frequency increases, achieving all these requirements becomes more and more a challenging because of the presence of the drain bonding wire. Indeed, as frequency increases, its inductance nature tends to isolate the intrinsic drain of the FET from outside load impedance. In practice, presenting a short circuit to the FET drain at RF and LO frequencies above 20 GHz appears as a quasi-impossible task. Because of this, the performances that can be achieved with a FET mixer in hybrid technology are necessarily limited even though performances of the FET itself are excellent. The device presented in this paper is able to overcome this problem owing to the integration of a decoupling capacitor directly between the drain and source metallisations. To our knowledge such a technique has never been used for mixers. On the other hand, it has been successfully applied to low noise amplifiers based on dual-gate cascode HEMT's, with the second gate grounded [1]. This device, directly loaded by a $50\text{-}\Omega$ standard impedance constitutes an elementary mixer cell being able to operate with a broad IF frequency bandwidth. Used with an additional output tuning network, in order to present at its drain a higher than $50\text{-}\Omega$ IF load impedance, it is expected to allow mixer operation with a substantial conversion gain improvement in comparison with usual HEMT's.

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II. DEVICE PROCESSING

The role of the integrated on-drain capacitor is to ground the HEMT drain as well as possible at RF and LO frequencies but not at IF frequency. It is clear that this second factor conditions the choice of the capacitance value, which has been fixed around 1 pF. Such a value is reasonable enough to permit the use of a $100\text{-}\Omega$ load resistance at 2 GHz IF frequency. This assertion is based on our experience in hybrid mixer design.

In order to allow a clear demonstration of the interest the new device, the drain capacitor processing has only been realized on one half of the wafer. This half has an integrated on-drain capacitor and the second half does not have. A complete extraction of the equivalent small signal circuits of each of the two halves of these two types of HEMT has been performed to check the similarity of their elements except for the drain-source capacitance [2].

The transistor has been realized on a double-quantum well InGaAs/AlGaAs/GaAs structure. Such a structure was chosen because it offers the advantage of a quasi square-shaped transconductance profile and therefore is particularly favorable to gate mixer operation. The layer was grown on a 2-in substrate in a RIBER 32 MBE system. After a $6000\text{-}\text{\AA}$ GaAs buffer were grown a $120\text{-}\text{\AA}$ $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ quantum well, a $30\text{-}\text{\AA}$ AlGaAs spacer, a Si delta doping plane ($4 \times 10^{12}\text{ cm}^{-2}$) a $50\text{-}\text{\AA}$ AlGaAs spacer, then a $120\text{-}\text{\AA}$ GaAs quantum well, a $30\text{-}\text{\AA}$ AlGaAs spacer, a Si delta doping plane ($3 \times 10^{12}\text{ cm}^{-2}$), an undoped AlGaAs layer and a $3 \times 10^{18}\text{ cm}^{-3}$ Si-doped GaAs cap layer. The Al content was 23%. The growth temperature was controlled by an infrared pyrometer to be 600°C for AlGaAs, 580°C for GaAs, and 520°C for the quantum wells, the spacers, and the doping planes so as to reduce Si segregation. The temperature was changed during the growth process.

Indium was introduced in the furthest quantum well. The higher velocity in InGaAs compared to GaAs will moderate the decrease in transconductance coming from the large gate channel separation and therefore ensure the required square-shaped profile. The grown layer was characterized by Van der Pauw measurements after removal of the cap layer. The room temperature results were respectively $7.7 \times 10^{12}\text{ cm}^{-2}$ and $3400\text{ cm}^2/\text{V.s}$ for the Hall electron density and mobility. At 77 K, $6 \times 10^{12}\text{ cm}^{-2}$ and $6300\text{ cm}^2/\text{V.s}$ were measured. The process starts with the realization of the transistor. The drain-integrated capacitor is realized next. MESA were etched chemically using $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ (1:1:200). The Ni/AuGe/Ni ohmic contacts were evaporated and annealed at 420°C for 40 s. The T-shape gate was realized on silicon

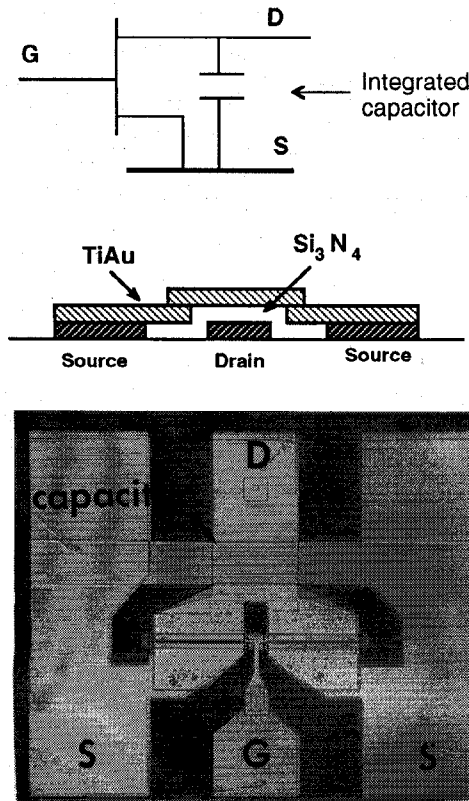


Fig. 1. Realization of the FET with integrated on-drain capacitor.

nitride. This layer was first deposited at 300°C by plasma. The 0.3 μm -gate was opened in the nitride by CF_4 . Then the cap layer was selectively etched on AlGaAs by a CCl_2F_2 plasma. Finally, the gate was deposited. Then a TiAu layer was deposited. This layer designs a waveguide compatible with Cascade probe measurements (Fig. 1). It is also the bottom capacitor electrode. The dielectric layer consists of 2500-Å thick silicon nitride. Its dielectric constant has been measured on test capacitors and equals about 7.5. The second metal layer is designed to realize the capacitor. Its value was estimated by S parameters extraction to be about 0.8 pF.

III. RESULTS AND DISCUSSION

The two types of devices were mounted in a low-loss microstrip test fixture with K connector terminations. In both cases, mixer measurements were carried out using, respectively 18 GHz, 16 GHz, and 2 GHz as RF, LO, and IF frequencies. The mixer measurement setup comprised two bias tees, a 10 dB proximity coupler for the RF and LO combination and a mechanical tuner placed just before the test fixture for the HEMT input matching at 18 GHz. The IF load was constituted either directly by the 50 Ω input of a spectrum analyser or by inserting before this one a low frequency mechanical tuner.

In the first case, i.e with a 50- Ω standard IF load, the peak value of the conversion gain was then about -3.5 dB. This result is in a good agreement with the estimate based on the well known analytical formula [3], [4]

$$G_c = \left(\frac{gm_{\max}}{8\pi F_{\text{RF}} C_{\text{GS}}} \right)^2 \frac{R_L}{R_{\text{in}}}$$

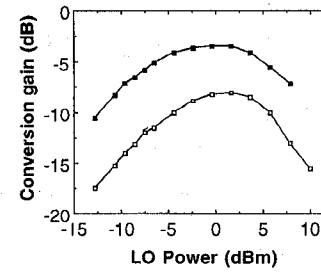


Fig. 2. Measured conversion gain (output loaded with 50 Ω): (—■—) with drain capacitor; (—□—) without drain capacitor.

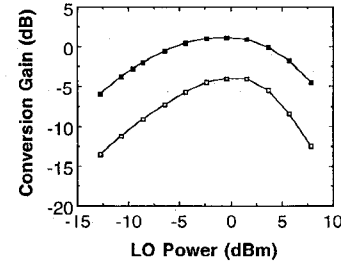


Fig. 3. Measured conversion gain (output tuned to IF): (—■—) with drain capacitor; (—□—) without drain capacitor.

taking:

$$gm_{\max} = 24 \text{ mS}, \quad C_{gs} = 0.12 \text{ pF}, \quad R_L = 50 \Omega, \\ R_{\text{in}} = 20 \Omega, \quad F_{\text{RF}} = 18 \text{ GHz}.$$

Given that this formula implies to an ideal treatment of the FET, it can be concluded that the result achieved from the HEMT with an integrated capacitor is nearly optimum.

On the other hand, it can be noted that the integrated-drain capacitor provides a 5-dB conversion improvement over the full LO power range (Fig. 2). This value is roughly in good agreement with our predictions carried out from simulations using MDS software from Hewlett-Packard.

In the second case, i.e with the IF tuner, a global improvement of all the results was found for the two devices but with the unchanged difference of about 5 dB to the advantage of the HEMT with its integrated capacitor (Fig. 3). The peak value of conversion gain reached by this device was then 1.4 dB.

IV. CONCLUSION

The present study has clearly demonstrated the interest of an integrated on-drain capacitor for an HEMT used in a mixer. It has been shown that this capacitor can compensate to a large extent for the counteracting effect inherent to a connection made with a bonding wire. This concept makes the realization of performant hybrid mixers possible and up to several tens of GHz constitutes an efficient alternative to a fully integrated circuit.

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REFERENCES

- [1] J. Wenger, P. Narozny, H. Dambkes, J. Splettstosser, and C. Werres, "Low-noise pseudomorphic dual-gate cascode HEMT's with extremely high gain," *IEEE Microwave and Guided Wave Lett.*, vol. 2, pp. 46-48, Feb. 1992.
- [2] G. Dambrine, A. Cappy, F. Héliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-36, pp. 1151-1159, 1988.
- [3] R. A. Pucel, D. Masse, and R. Bera, "Performance of MESFET mixers at X-band," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-24, pp. 351-360, 1988.
- [4] S. Maas, "Design and performance of a 45-GHz HEMT mixer," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-34, pp. 799-803, 1986.